

FIG. 1

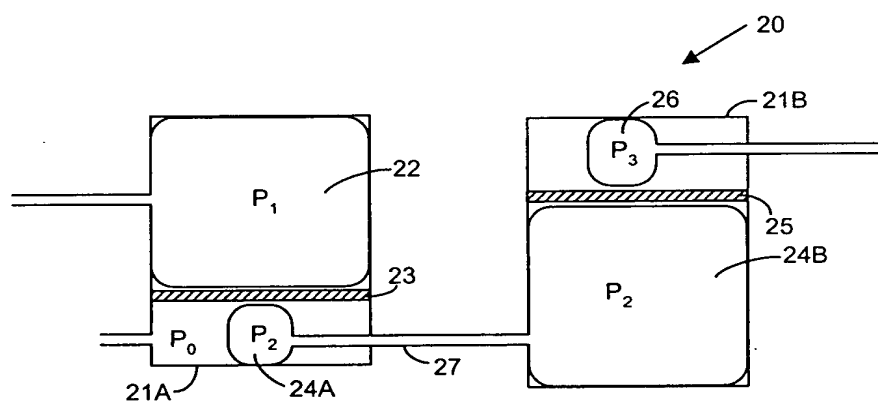


FIG. 2

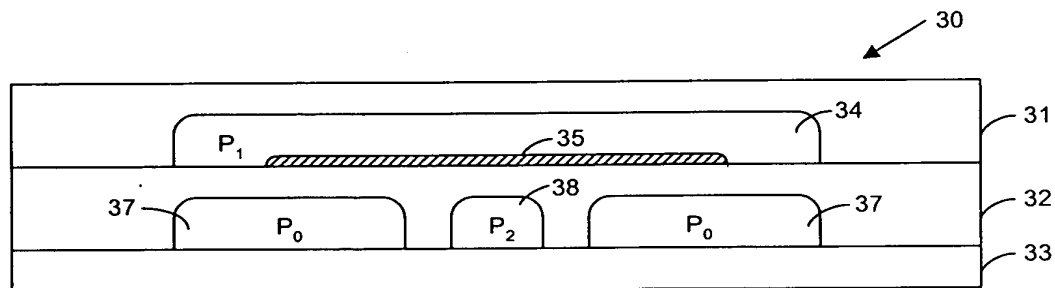
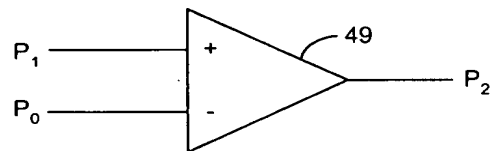
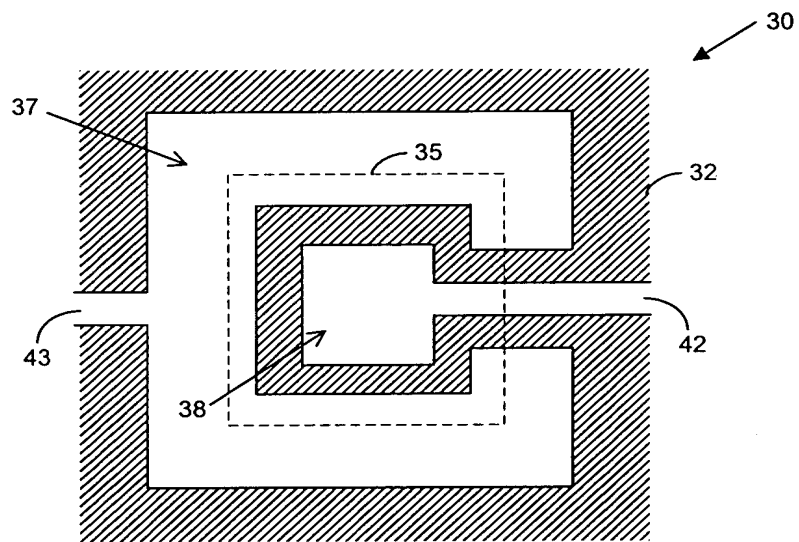
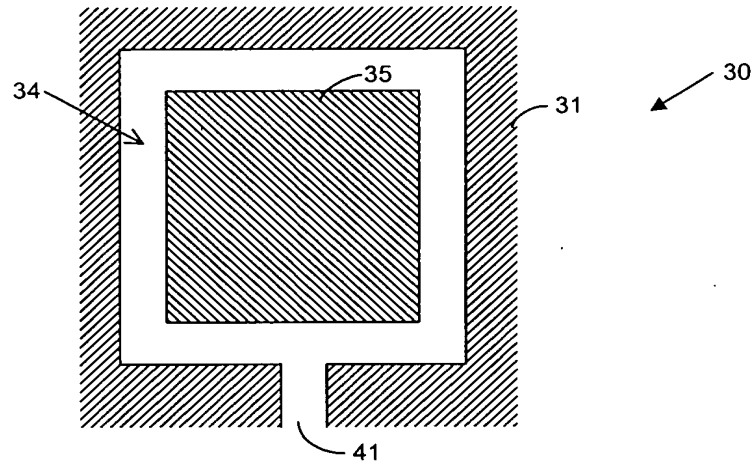


FIG. 3

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FOOTPRINT 26E56660



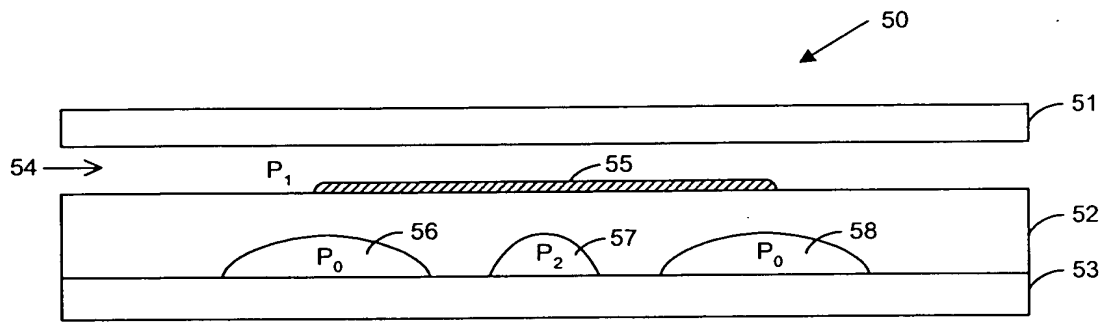


FIG. 5A

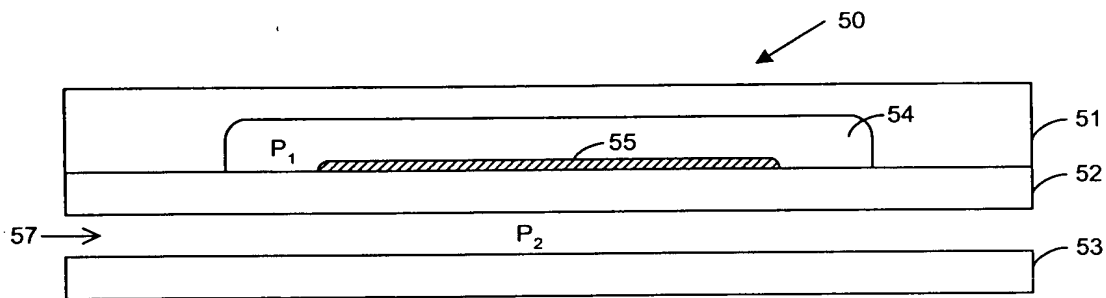


FIG. 5B

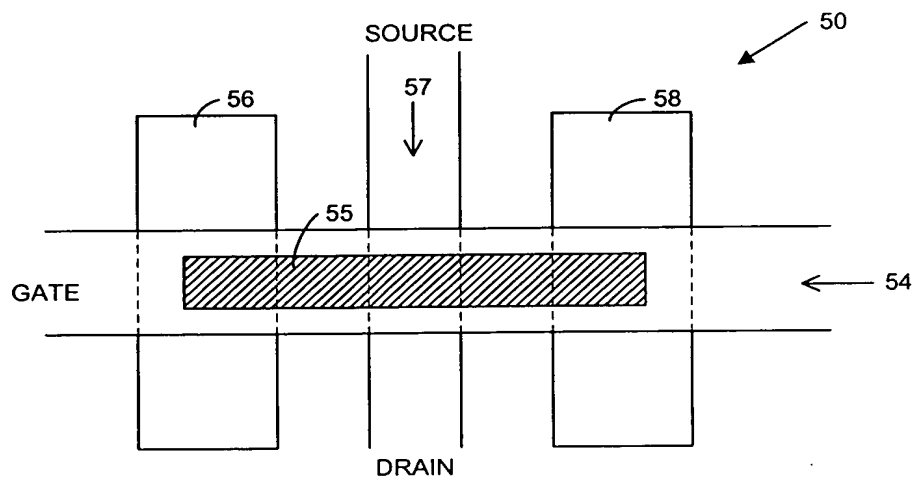


FIG. 6

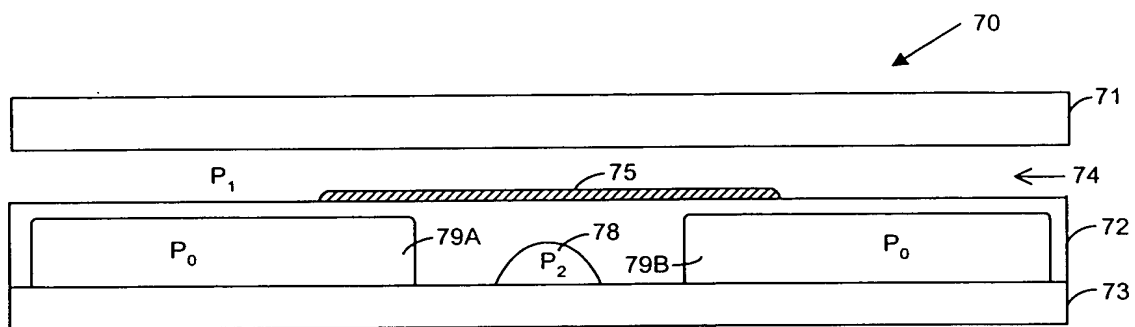


FIG. 7A

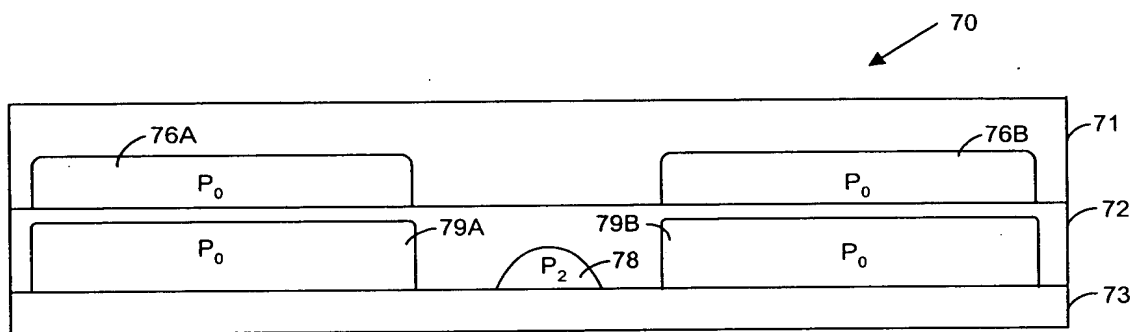


FIG. 7B

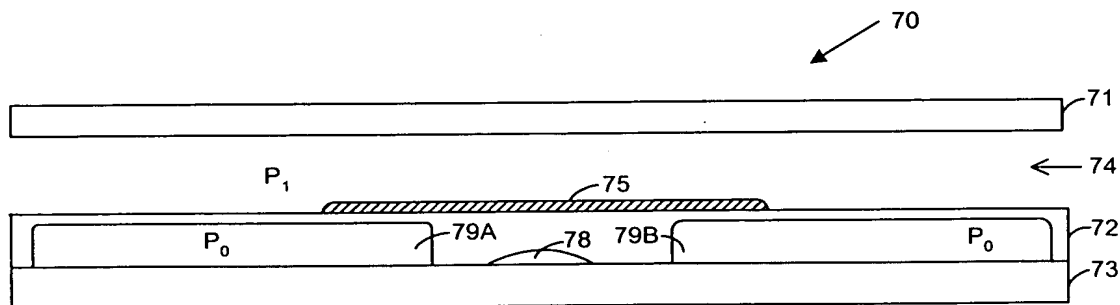


FIG. 7C

Diagram illustrating a cross-sectional view of a semiconductor device 70. The device features a central channel region 78, flanked by a SOURCE region on the left and a DRAIN region on the right. A gate structure 74 is positioned over the channel region, with gate electrodes 76A and 76B on either side. A gate insulating layer 75 is located above the gate electrodes. The device is surrounded by a substrate 77.

This cross-sectional view shows a substrate with a trench. A gate structure, labeled 80, is positioned above the trench. The gate structure includes a gate dielectric layer 81 and a gate electrode 82. The gate electrode 82 is divided into three regions: 89A, 89B, and 89C. The gate electrode 82 is surrounded by a gate sidewall 83. The gate sidewall 83 is divided into three regions: 84, 85, and 86. The gate sidewall 84 is located on the left side of the trench, the gate sidewall 85 is located on the right side of the trench, and the gate sidewall 86 is located on the top of the trench. The gate sidewall 84 is labeled with  $P_1$ , the gate sidewall 85 is labeled with  $P_2$ , and the gate sidewall 86 is labeled with  $P_0$ . The gate sidewall 84 is also labeled with 89A, the gate sidewall 85 is labeled with 89B, and the gate sidewall 86 is labeled with 89C. The gate sidewall 84 is also labeled with 88, the gate sidewall 85 is labeled with 88, and the gate sidewall 86 is labeled with 88.

FIG. 8

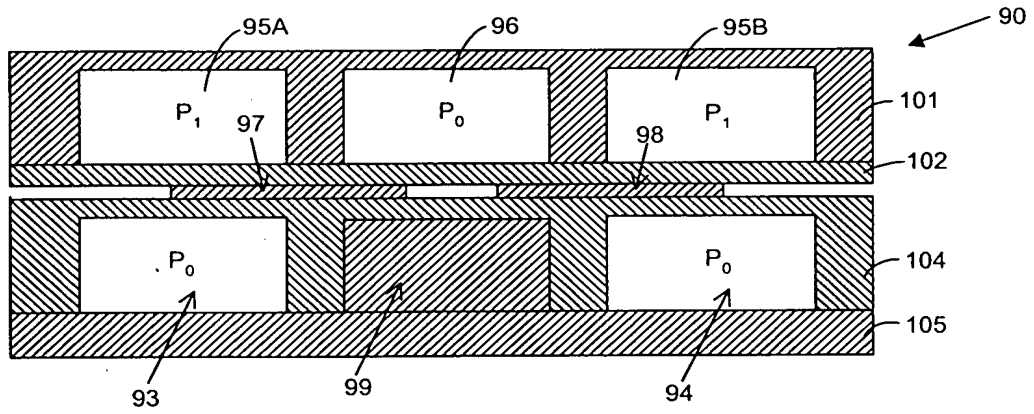


FIG. 9A

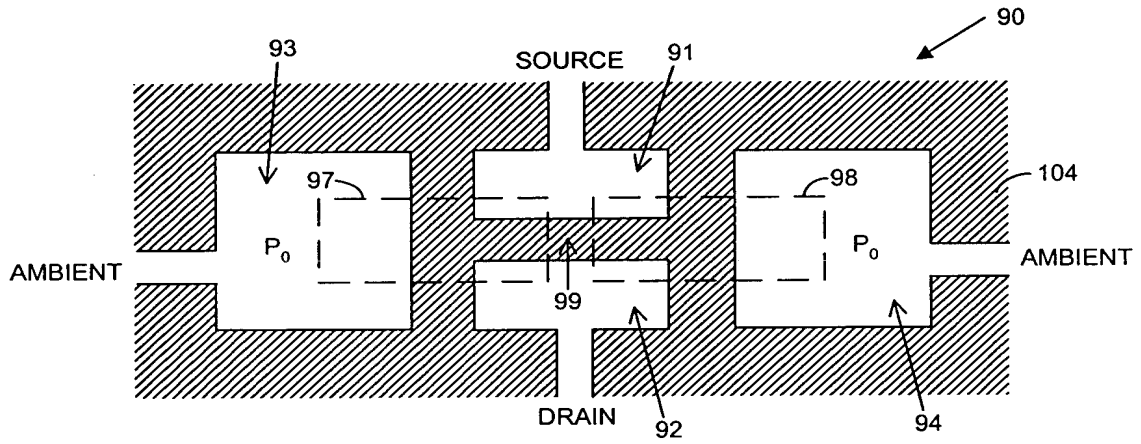


FIG. 9B

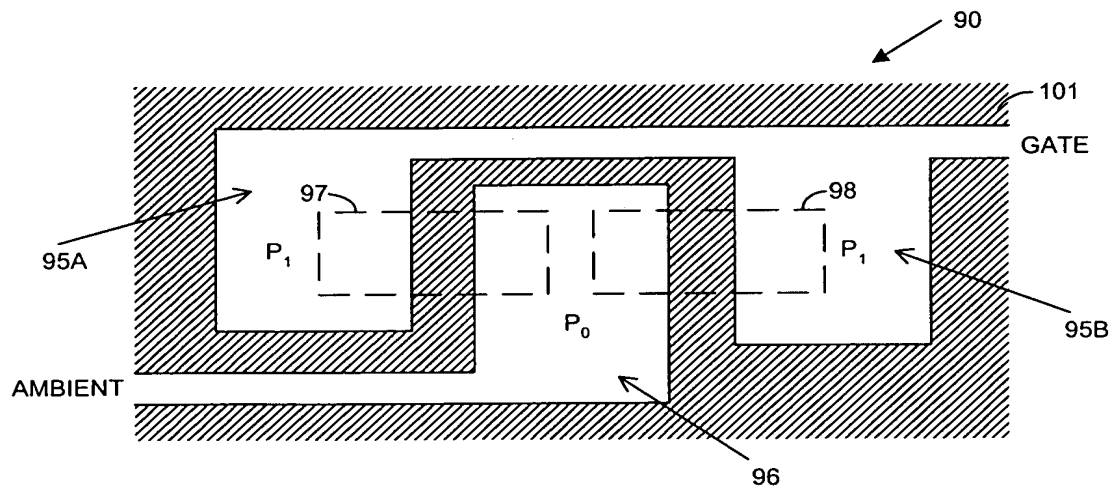


FIG. 9C

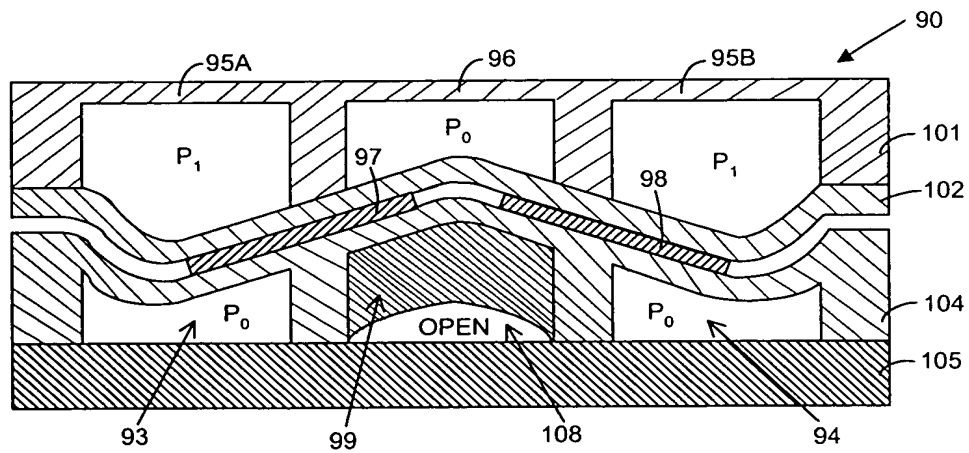


FIG. 9D

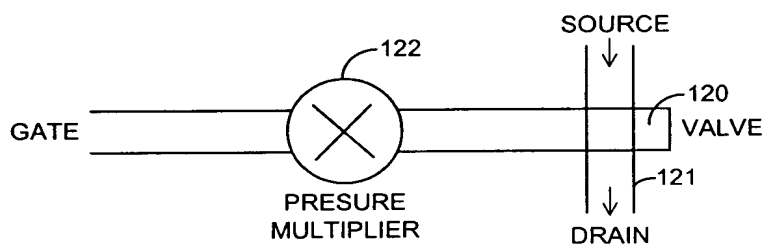


FIG. 10



FIG. 11A



FIG. 11B



FIG. 11C



FIG. 11D

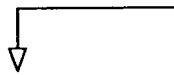


FIG. 11E



FIG. 11F

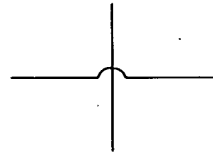


FIG. 11G

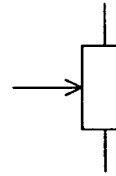


FIG. 11H

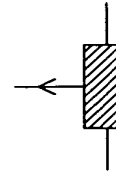


FIG. 11I

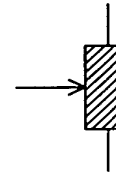


FIG. 11J

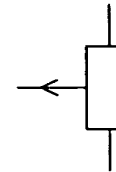


FIG. 11K



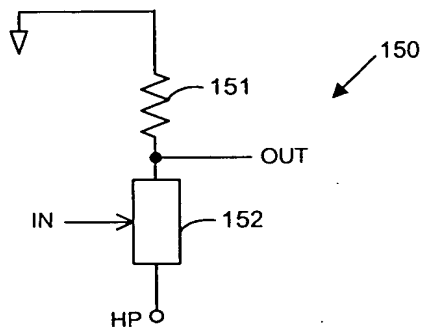


FIG. 12A

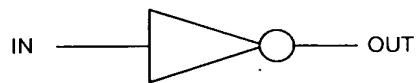


FIG. 12B

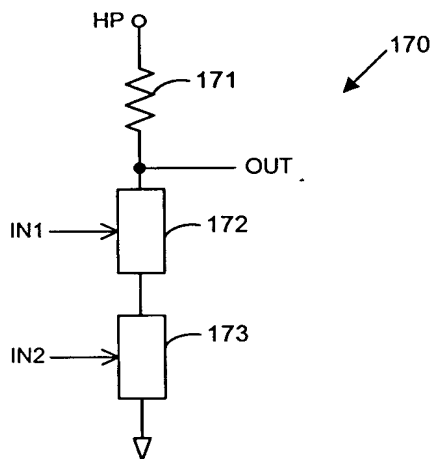


FIG. 12C

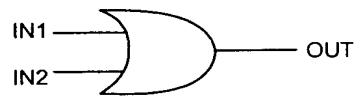


FIG. 12D

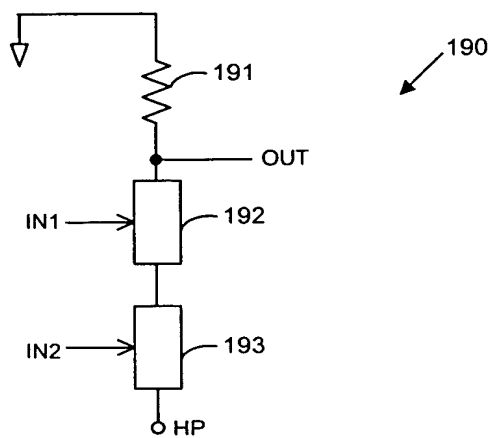


FIG. 12E

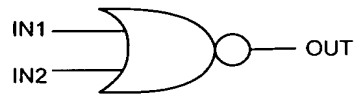


FIG. 12F

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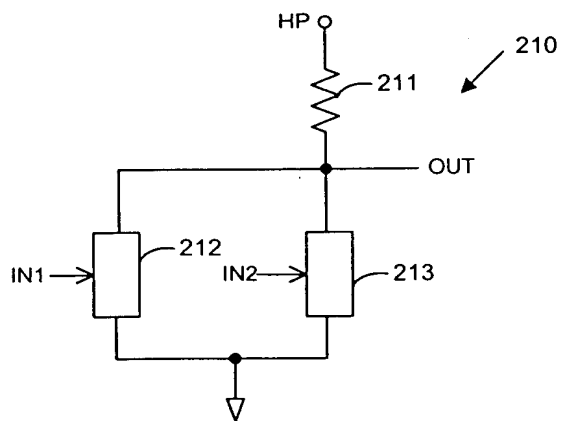
[illegible]

FIG. 12G

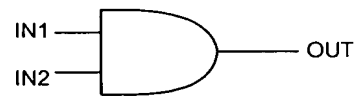


FIG. 12H

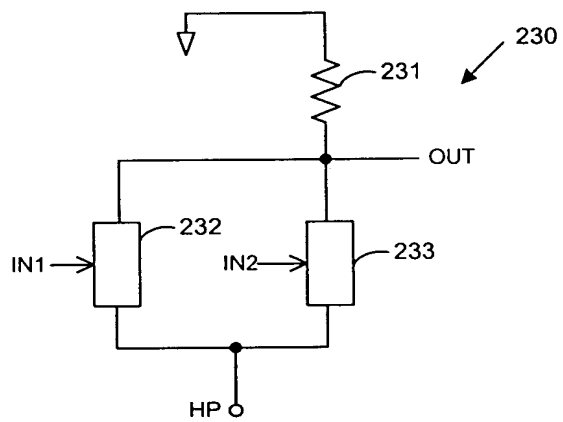


FIG. 12I

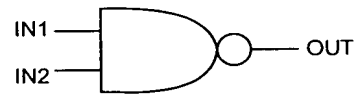


FIG. 12J

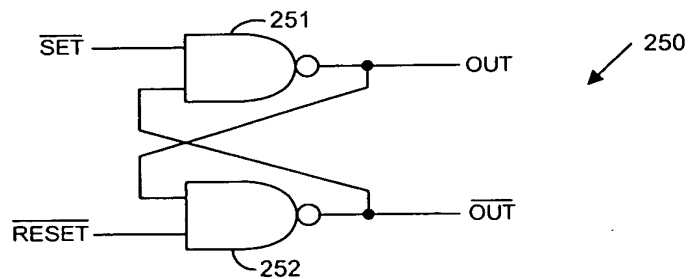


FIG. 13

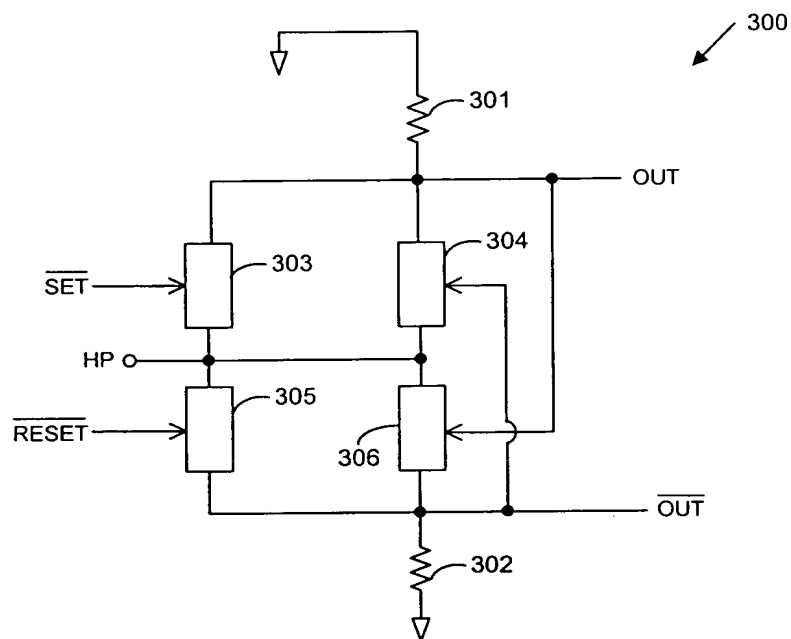


FIG. 14A

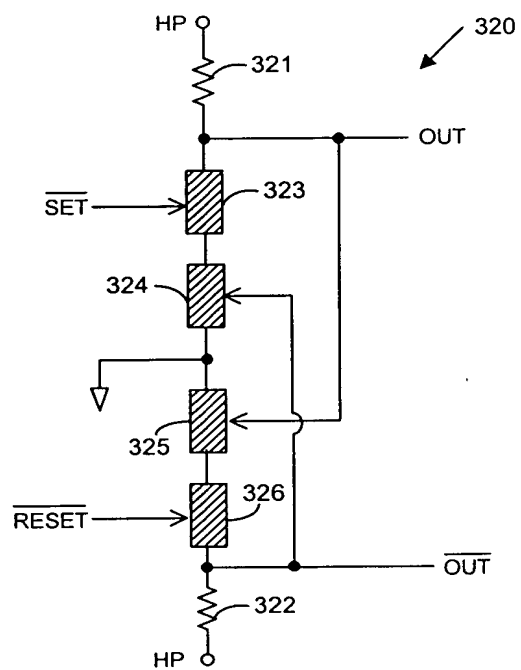


FIG. 14B

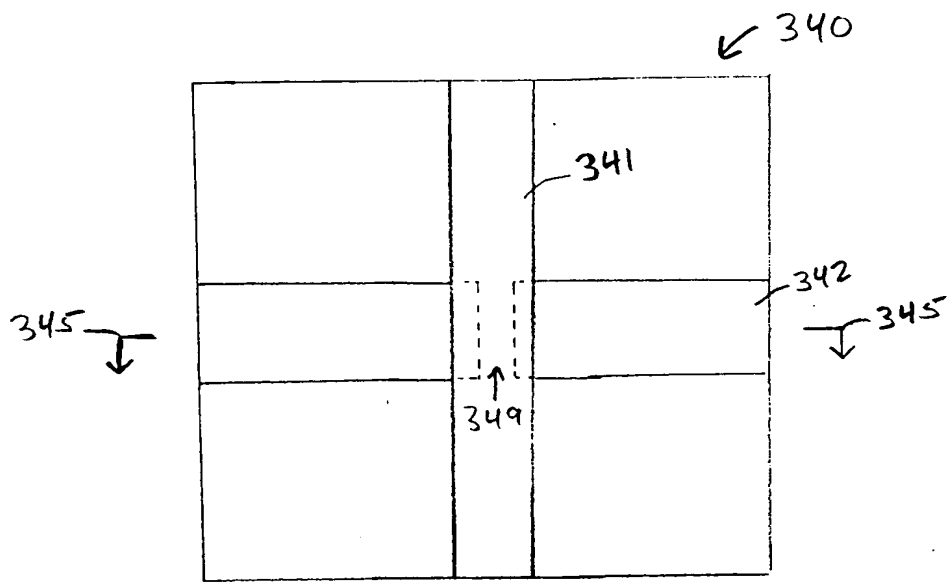


FIG. 15A

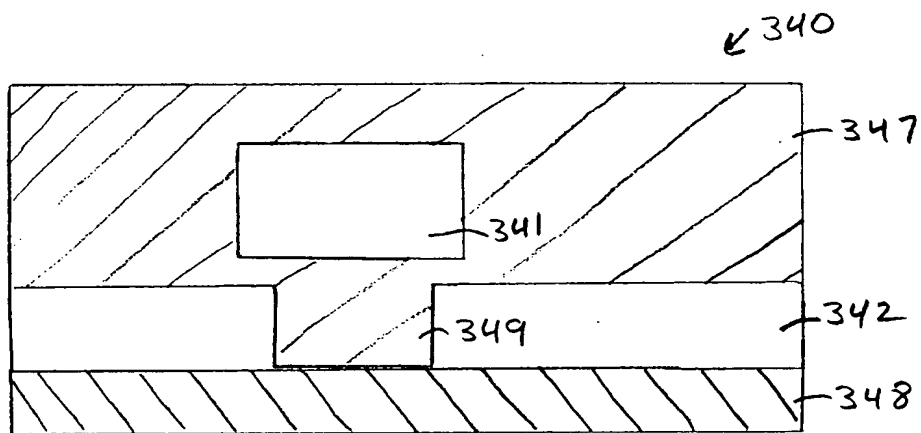


FIG. 15B

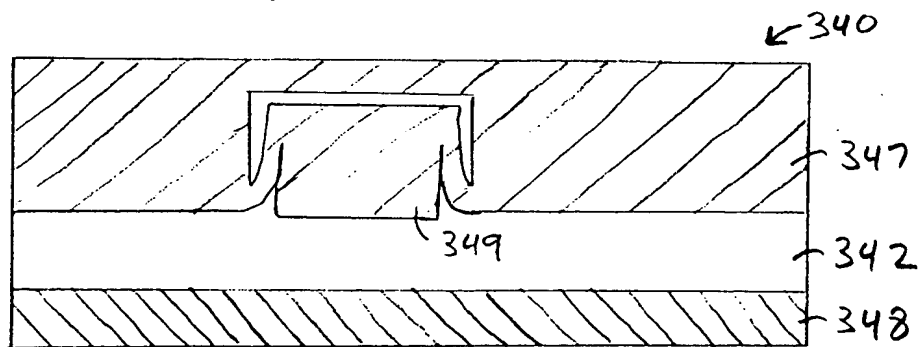


FIG. 15C

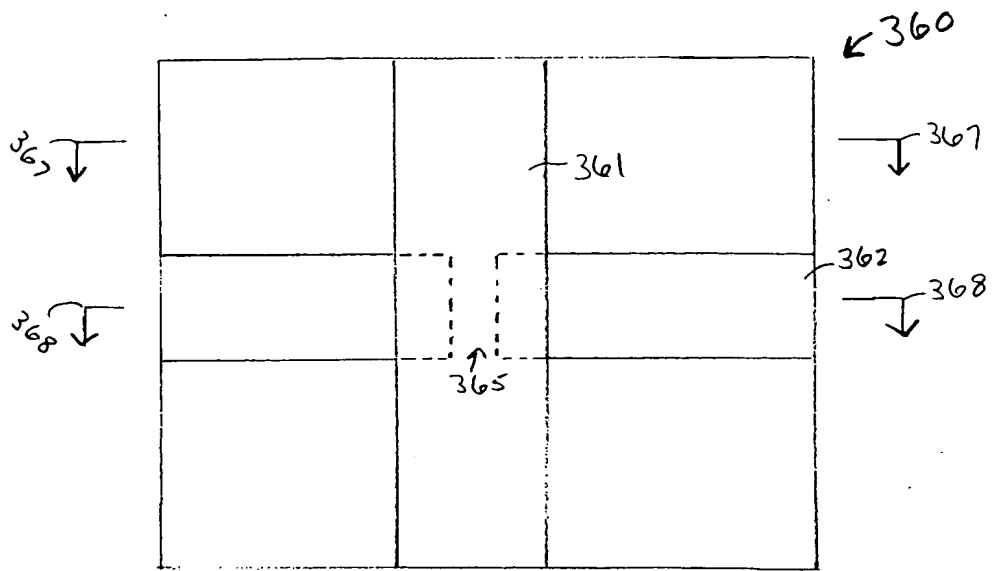


FIG. 15 D

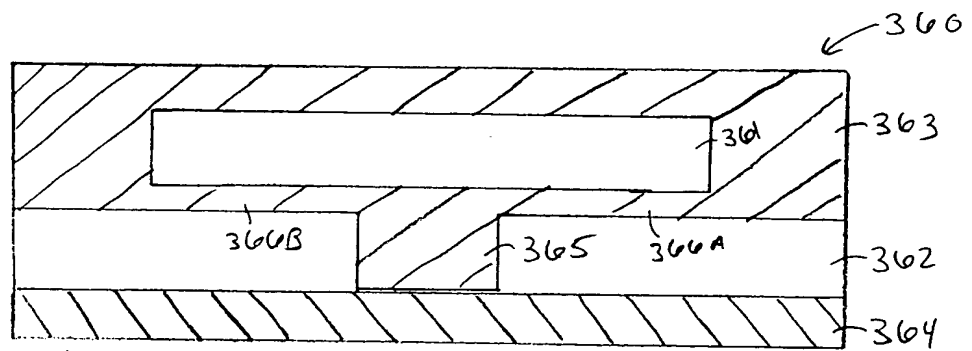


FIG. 15 E

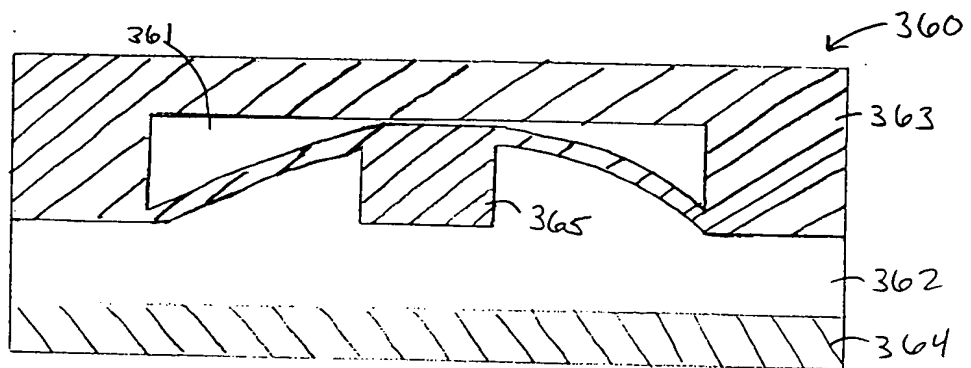


FIG. 15 F

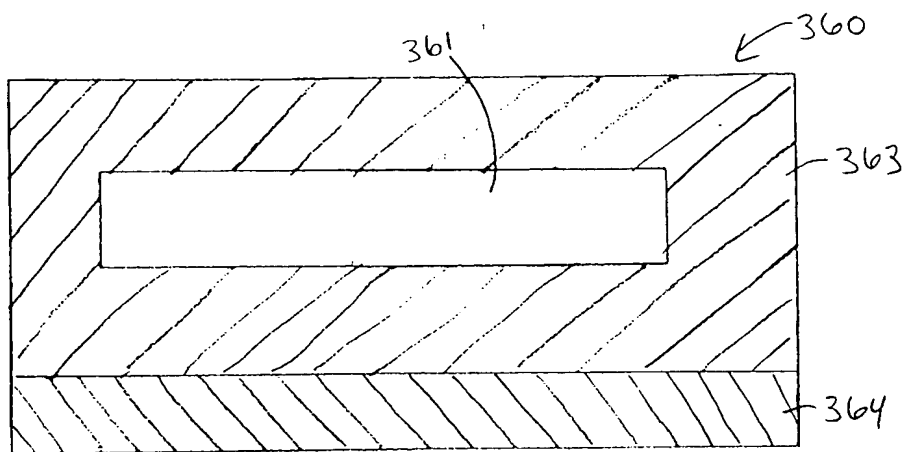


FIG. 15G

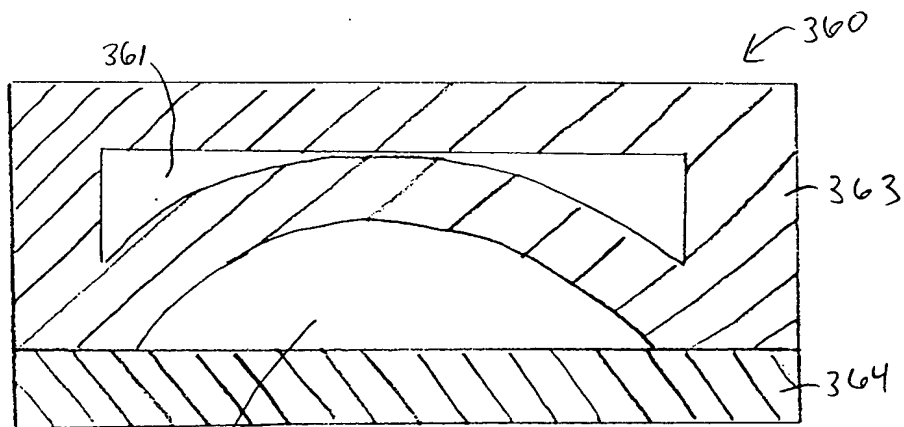
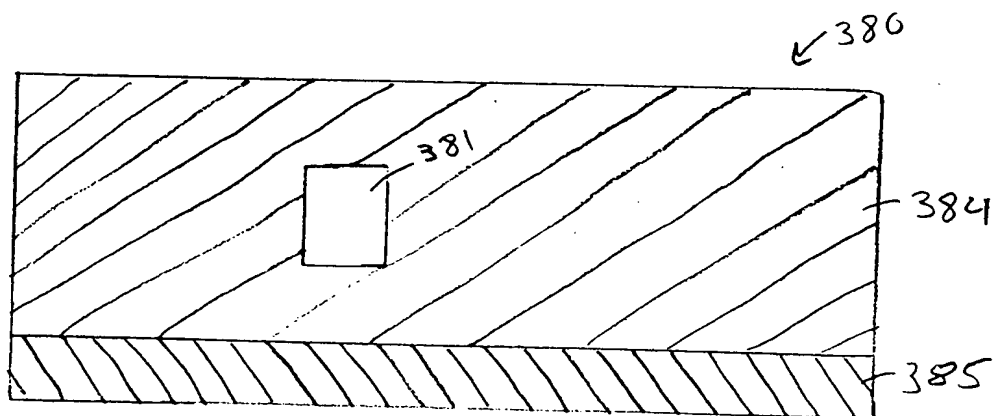
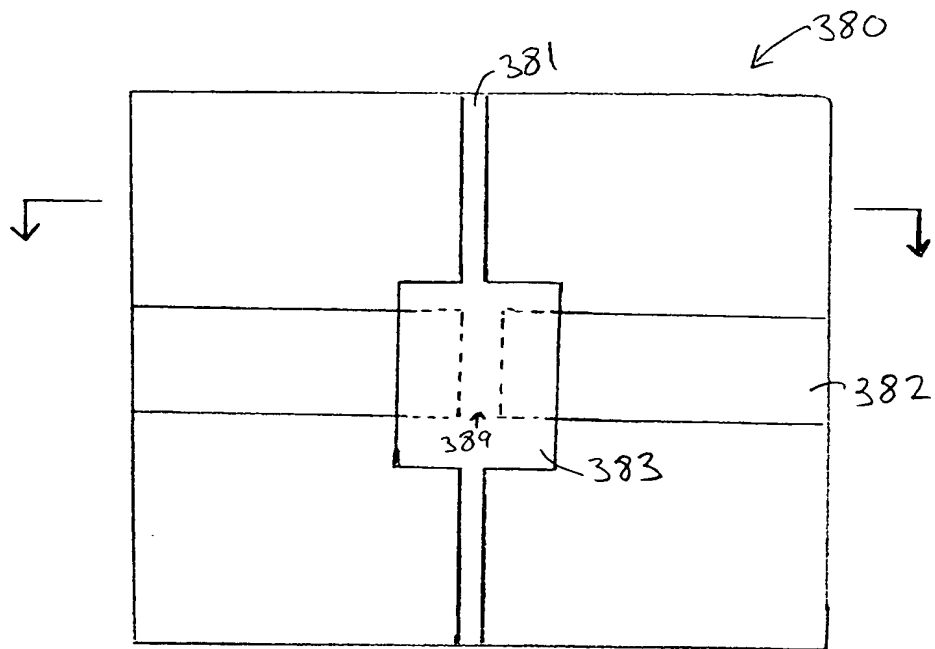


FIG. 15H

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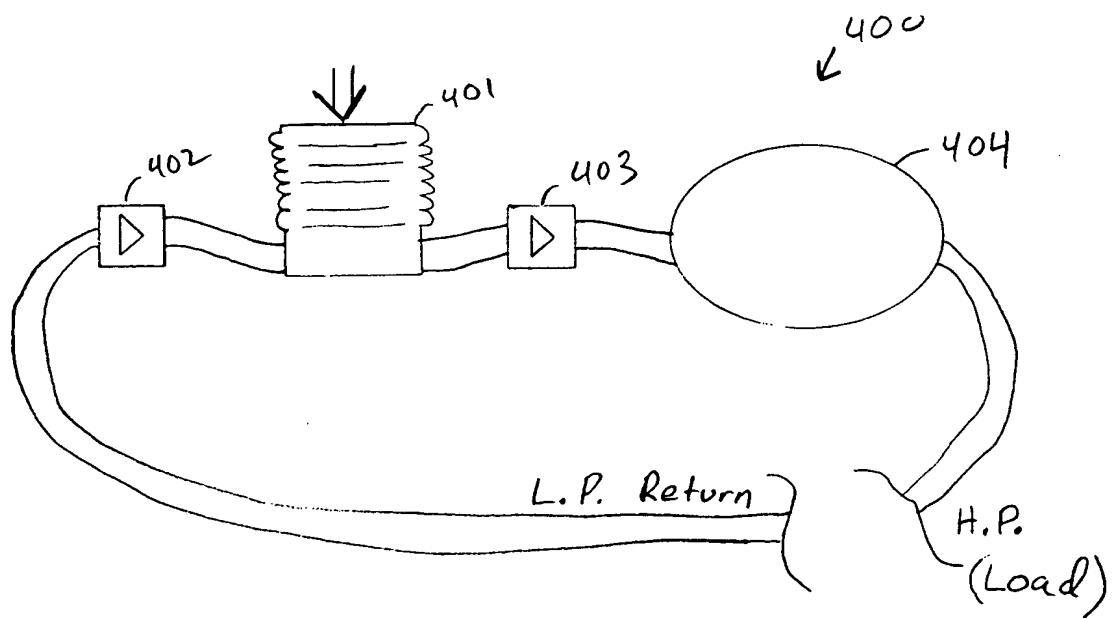


FIG. 16 (Prior art)

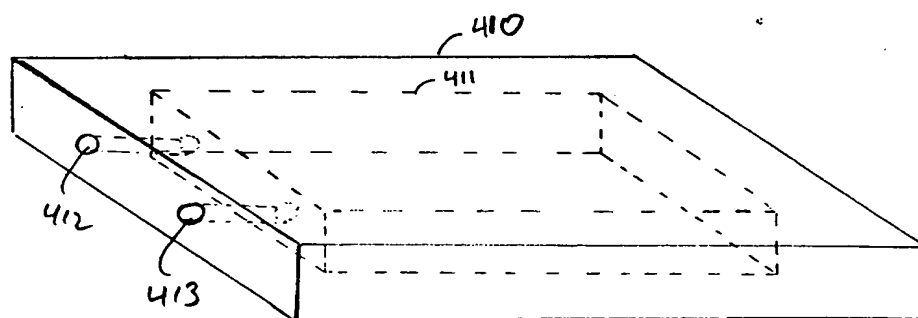


FIG. 17A



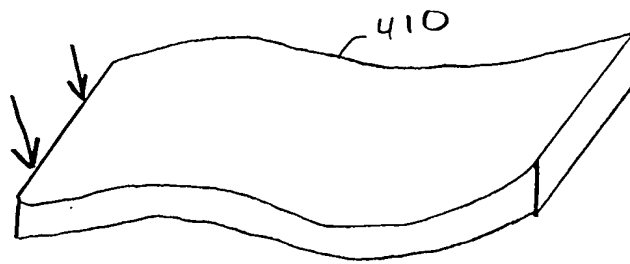


FIG. 17B

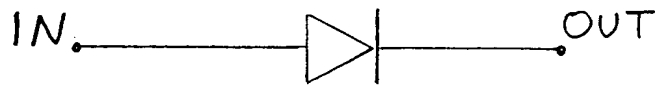


FIG. 18

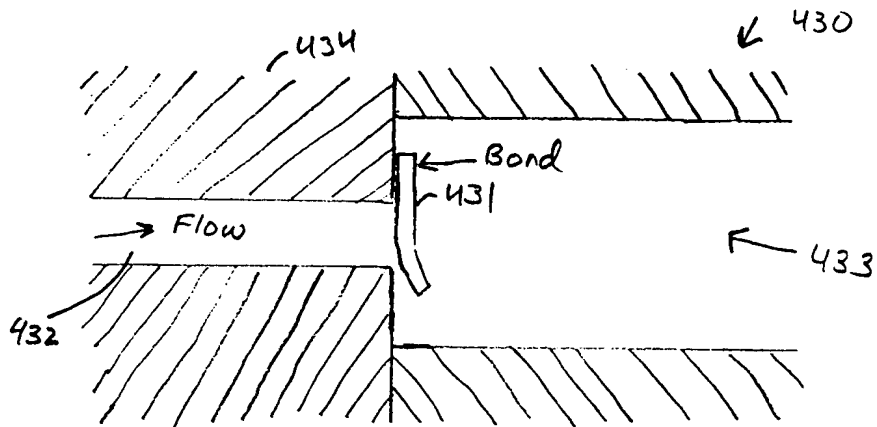


FIG. 19 (Prior art)

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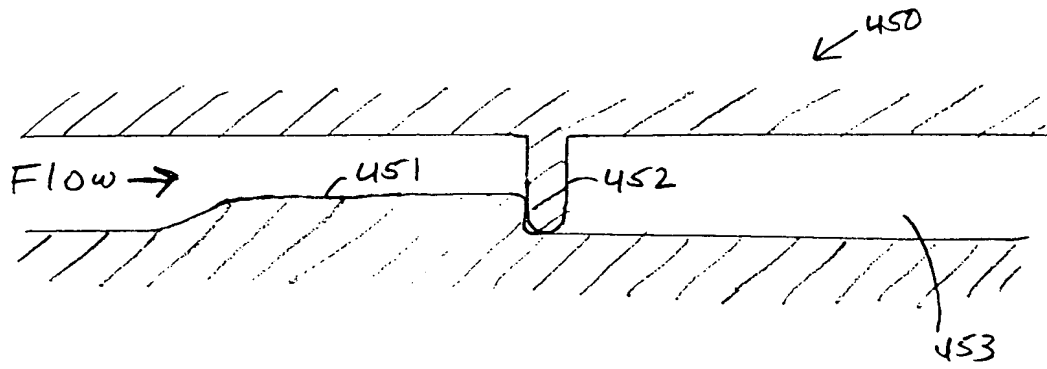


FIG. 20A

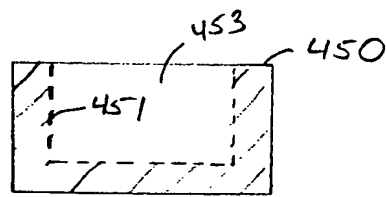


FIG. 20B

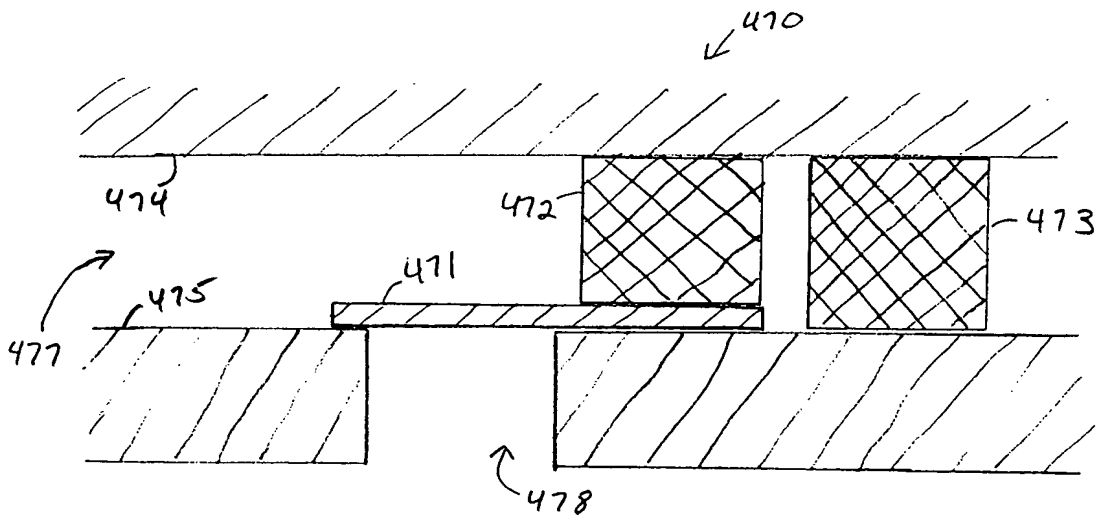


FIG. 21

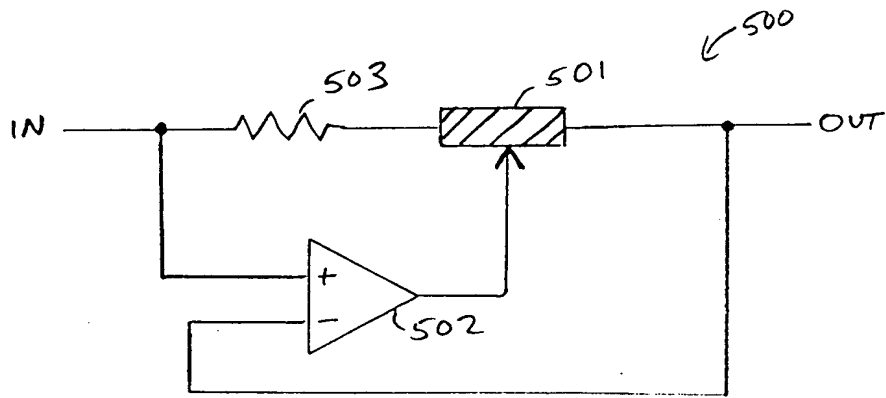


FIG. 22

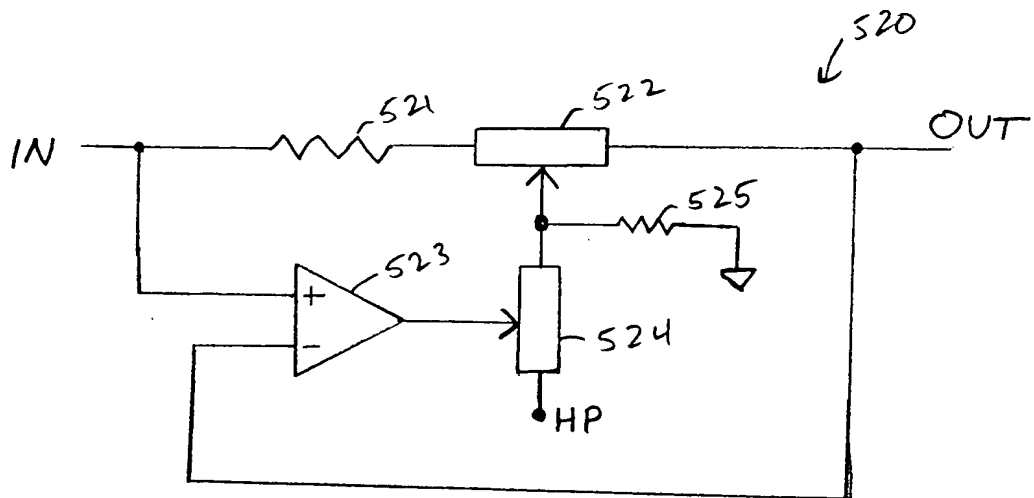


FIG. 23

FIG. 22

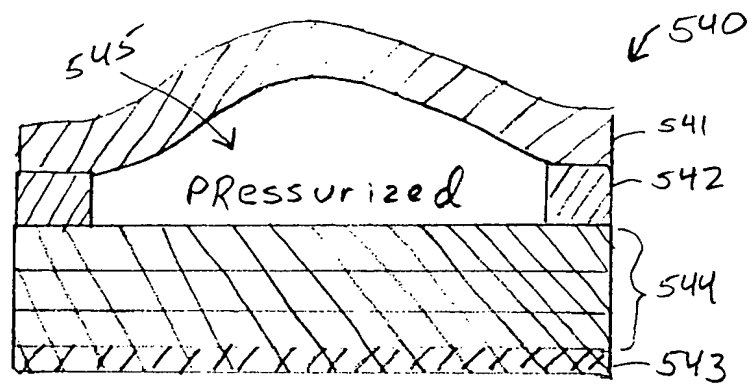


FIG. 24



FIG. 25A

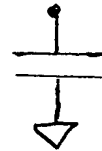


FIG. 25B

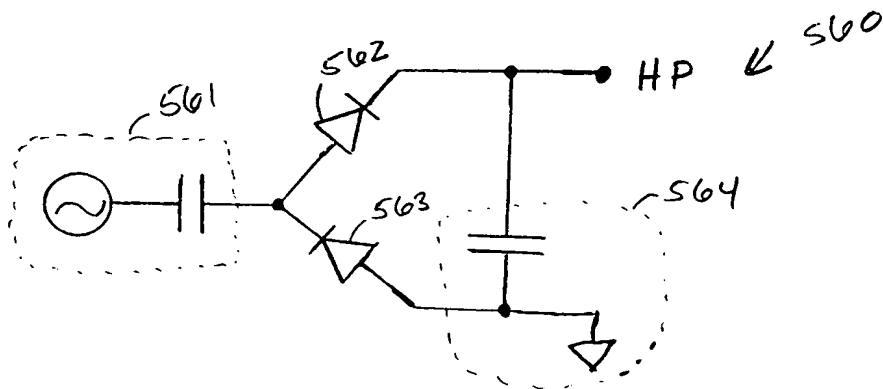


FIG. 26

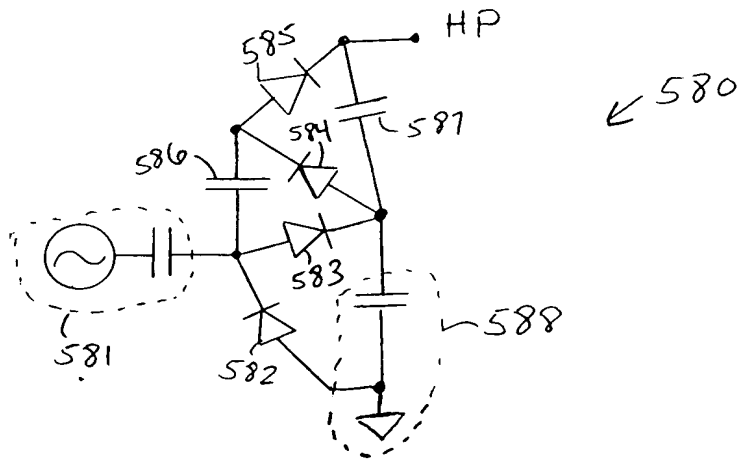


FIG. 27

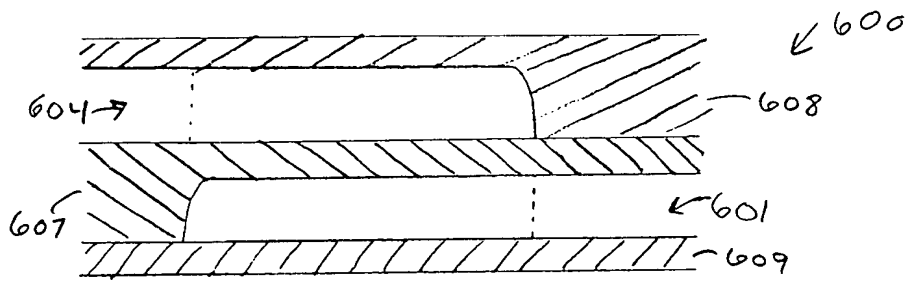


FIG. 28

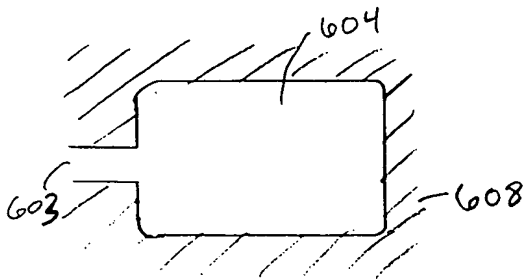


FIG. 29A

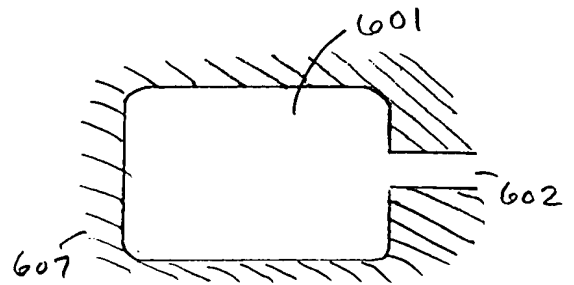


FIG. 29B

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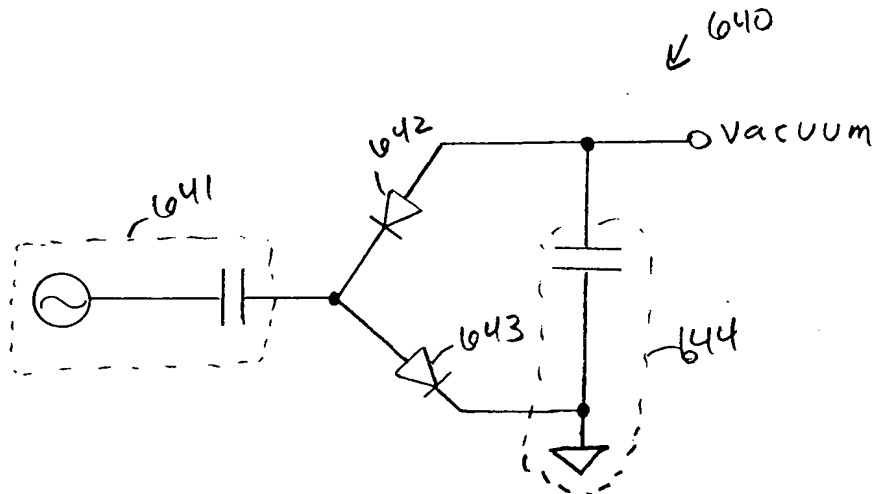


FIG. 30

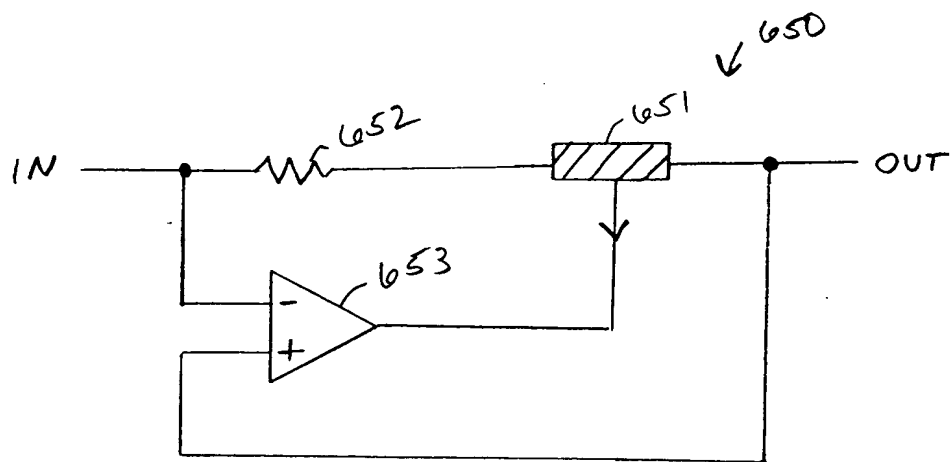


FIG. 31

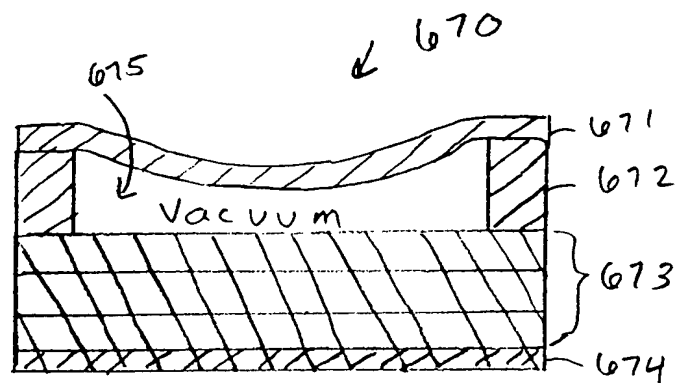


FIG. 32

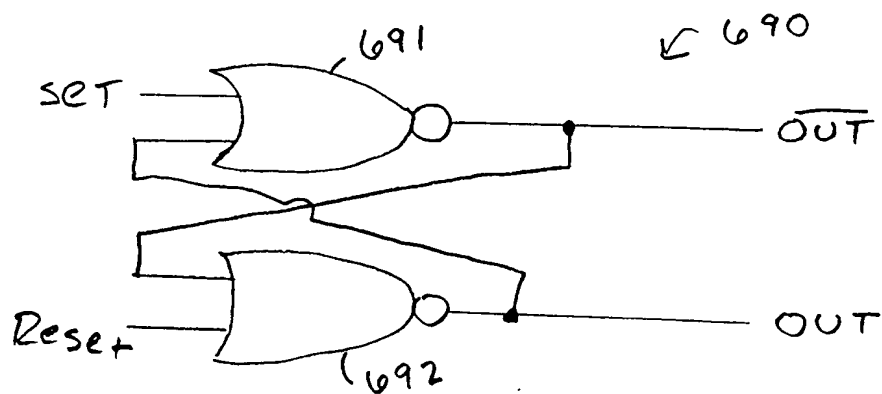


FIG. 33

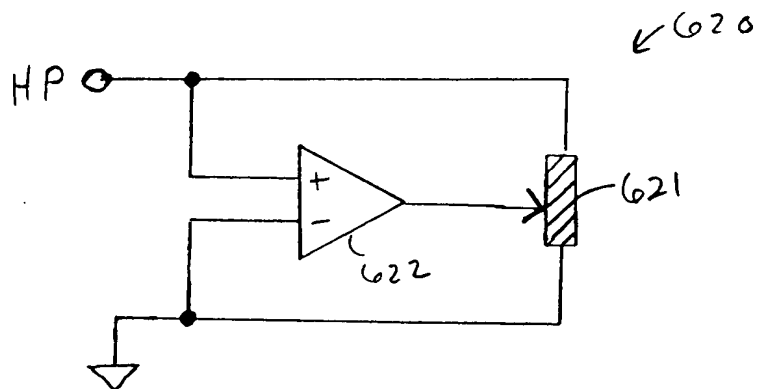


FIG. 34

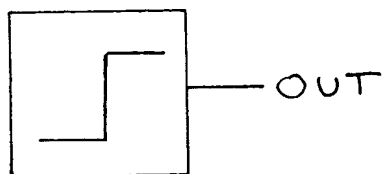


FIG. 35A

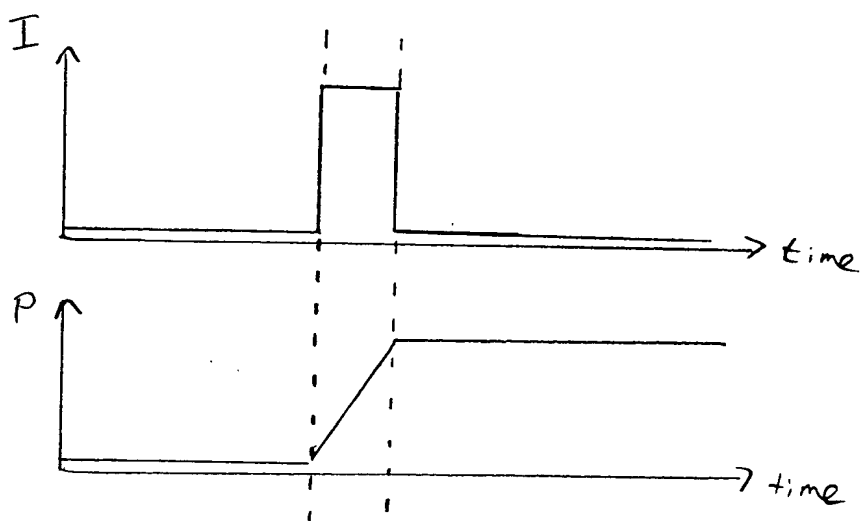


FIG. 35B

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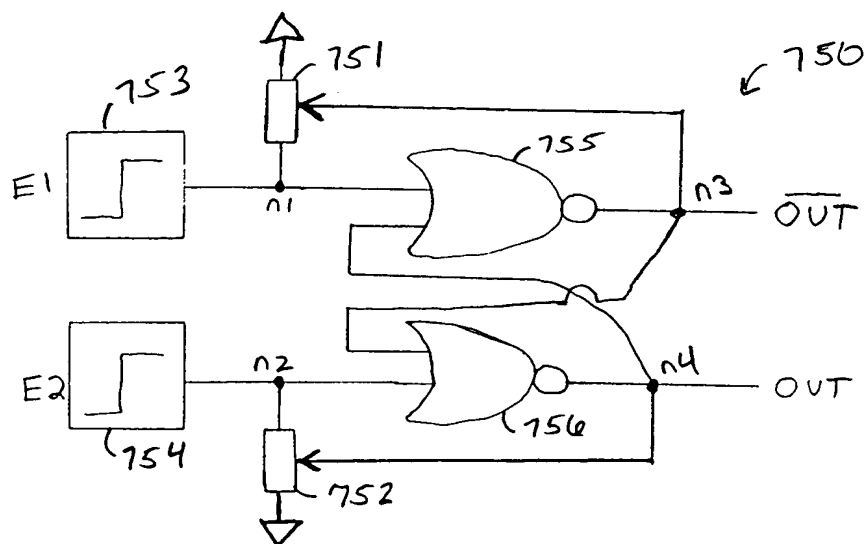


FIG. 36A

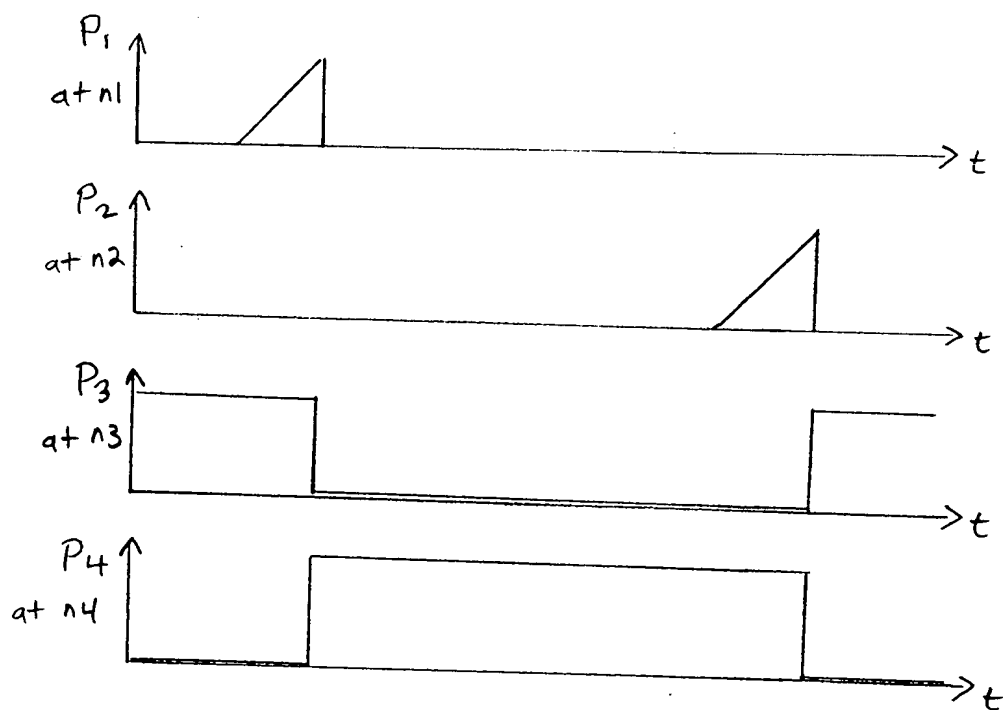


FIG. 36B

00000000 112601



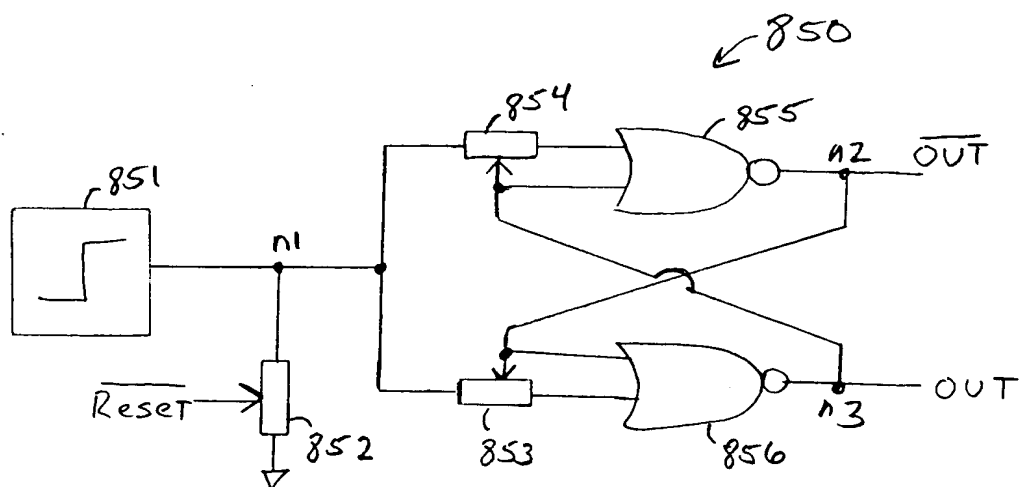
[illegible]

FIG. 38

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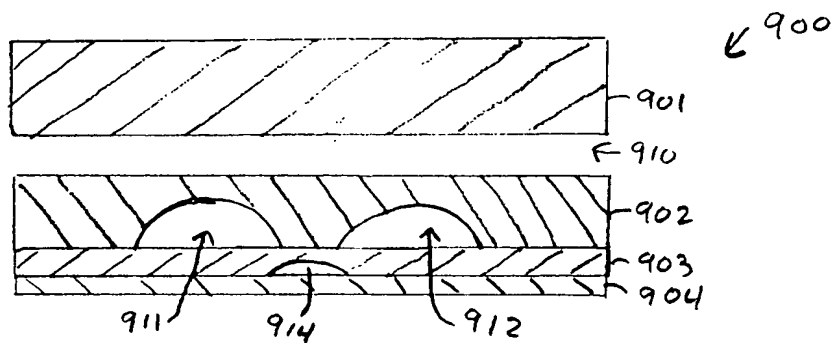


FIG. 39A

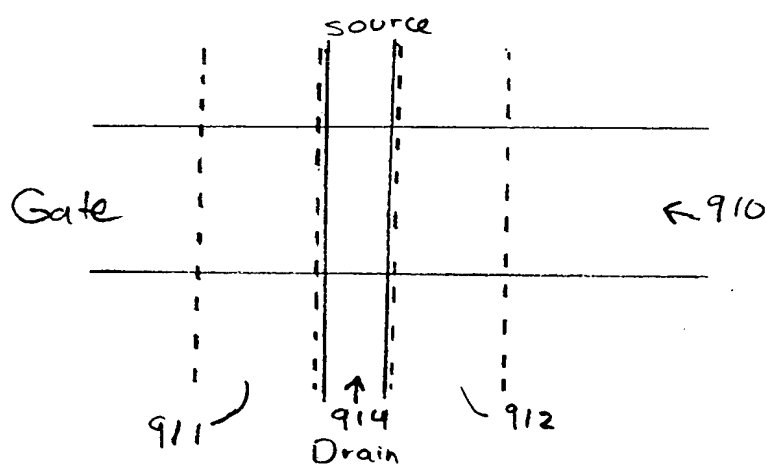


FIG. 39B

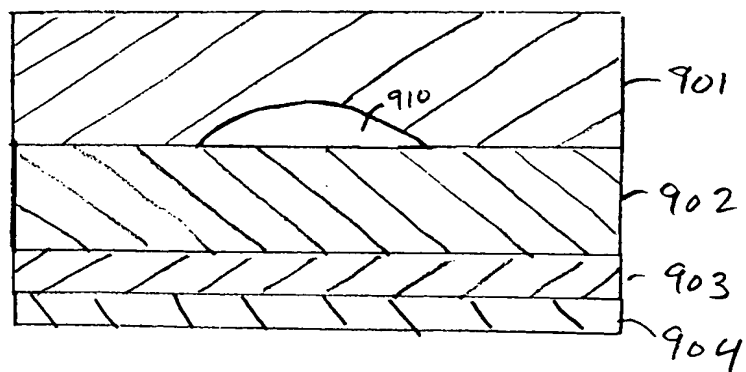


FIG. 39C

